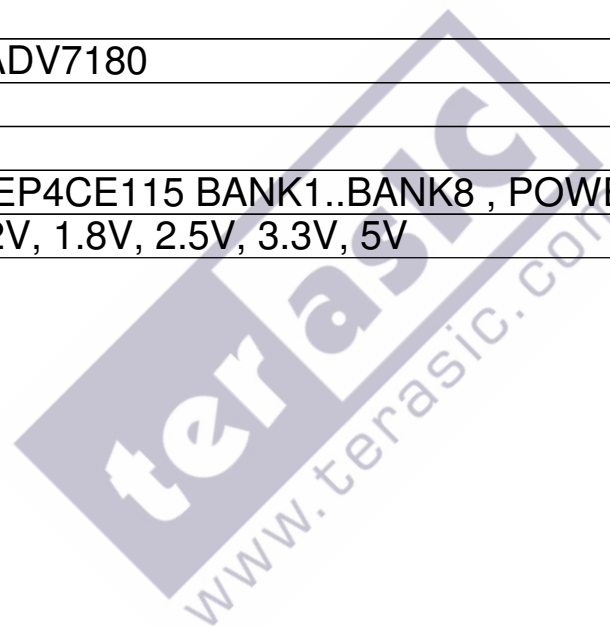

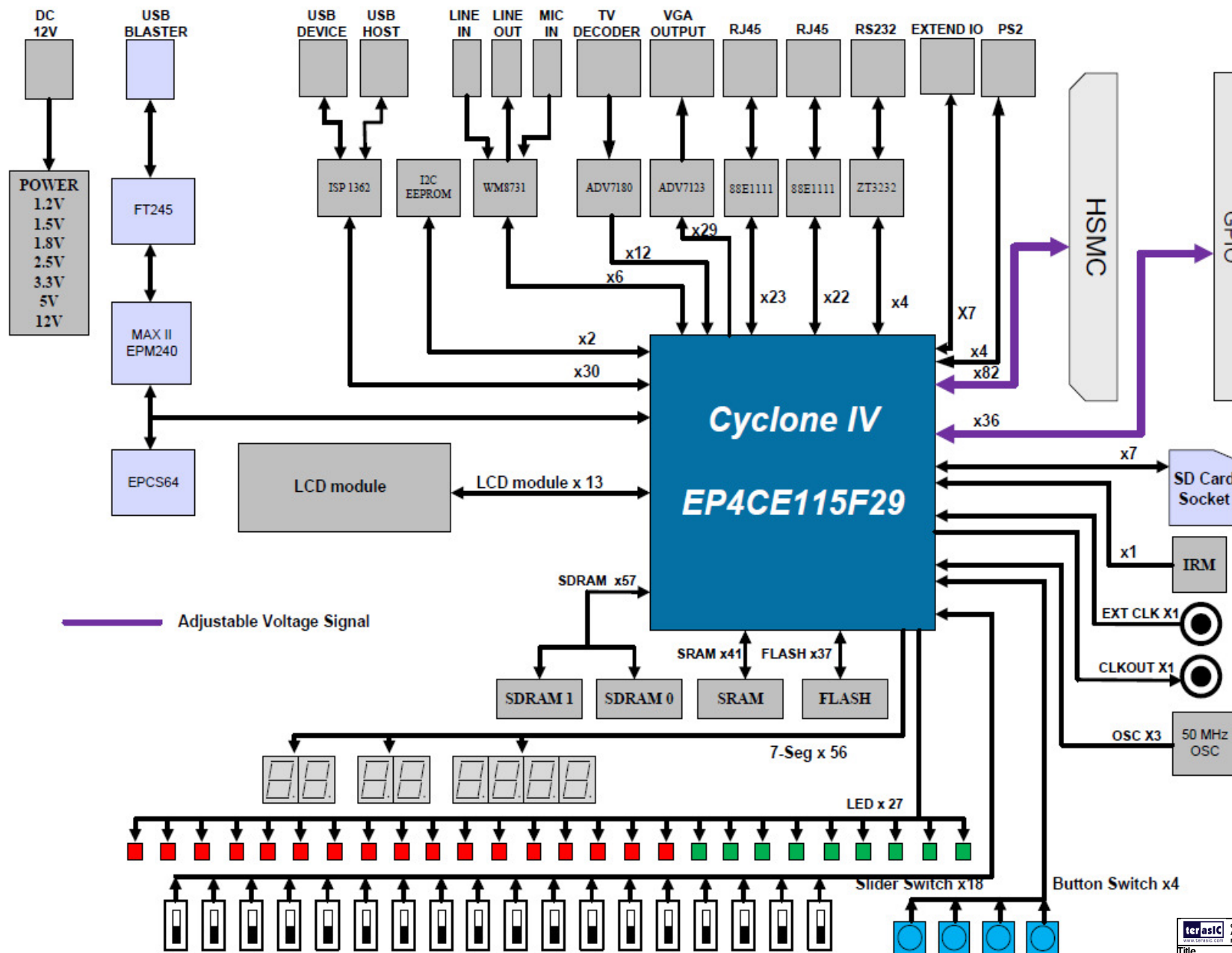


# ALTERA Cyclone IV Development & Education Board (DE2-115)

| SCHEMATIC     | CONTENT   | PAGE    |
|---------------|---|---------|
| 01 TOP        | Cover Page, Placement, TOP                                | 01 ~ 03 |
| 02 MEMORY     | SDRAM , SRAM , FLASH , SD CARD                            | 04 ~ 06 |
| 03 DISPLAY    | LCD , LED , 7SEGMENT                                      | 07 ~ 08 |
| 04 IN/OUT     | CLOCK, IrDA, PS2 , RS232 , BUTTON , SWITCH , HSMC, EEPROM | 09 ~ 14 |
| 05 ETHERNET   | 88E1111   | 15 ~ 16 |
| 06 VIDEO      | ADV7123, ADV7180  | 17 ~ 18 |
| 07 AUDIO      | WM8731  | 19      |
| 08 USB DEVICE | ISP1362   | 20      |
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| 10 POWER      | POWER 1.2V, 1.8V, 2.5V, 3.3V, 5V                          | 26 ~ 27 |






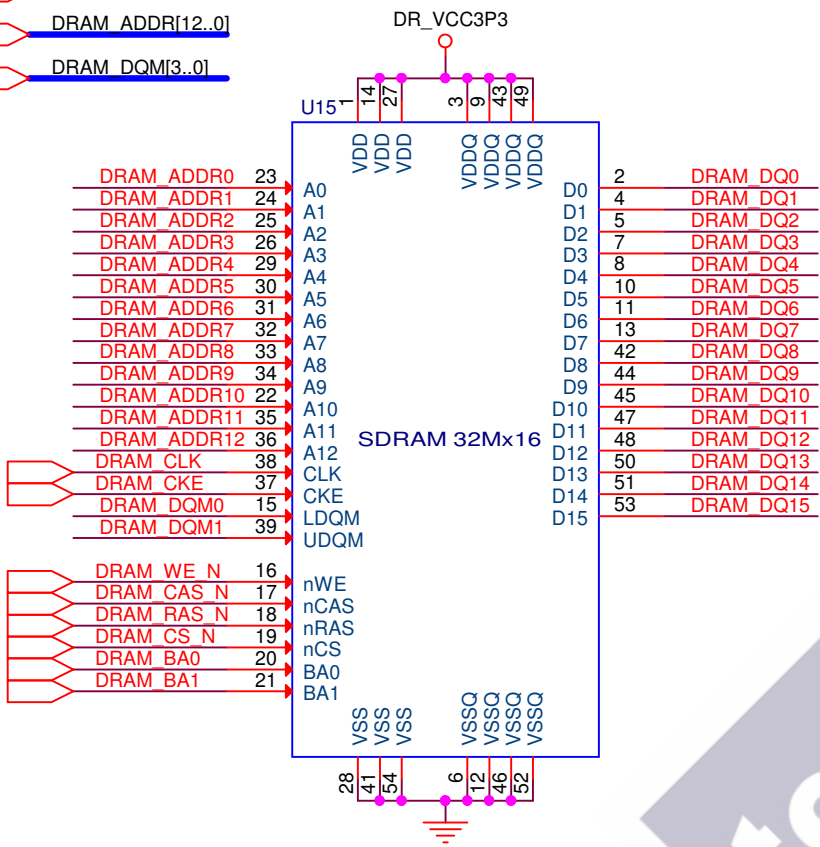
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| Title  |                            |               |
| <b>DE2-115 Main Board</b>  |                            |               |
| Size   | Document Number            | Rev           |
| B  | COVER PAGE                 | B             |
| Date:  | Friday, September 24, 2010 | Sheet 1 of 27 |



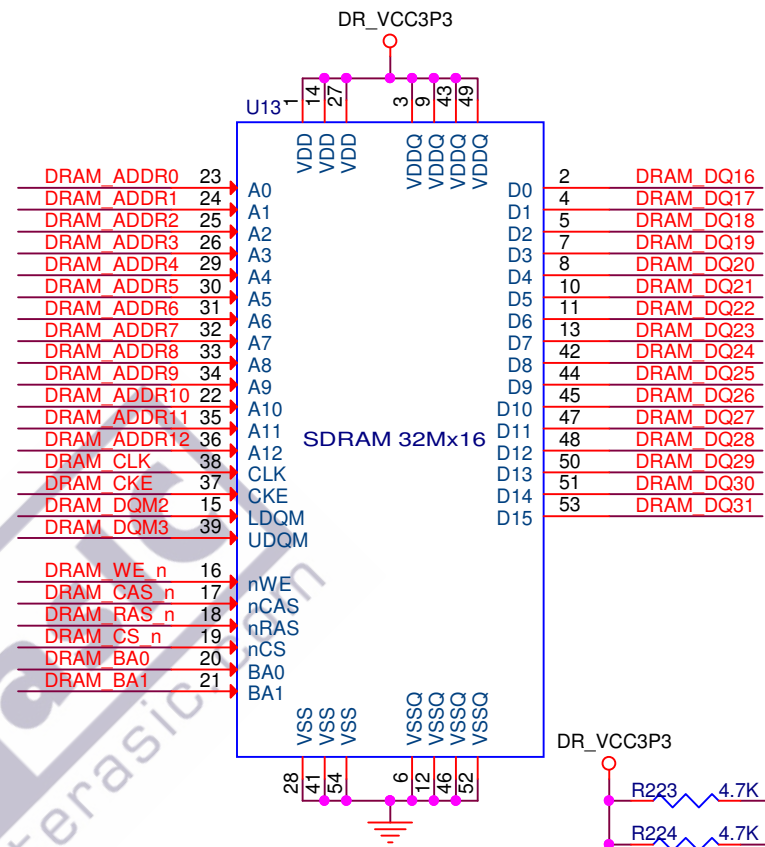
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| Title   |                            |               |
| DE2-115 Main Board  |                            |               |
| Size  | Document Number            | Rev           |
| B   | PLACEMENT                  | B             |
| Date:   | Friday, September 24, 2010 | Sheet 2 of 27 |



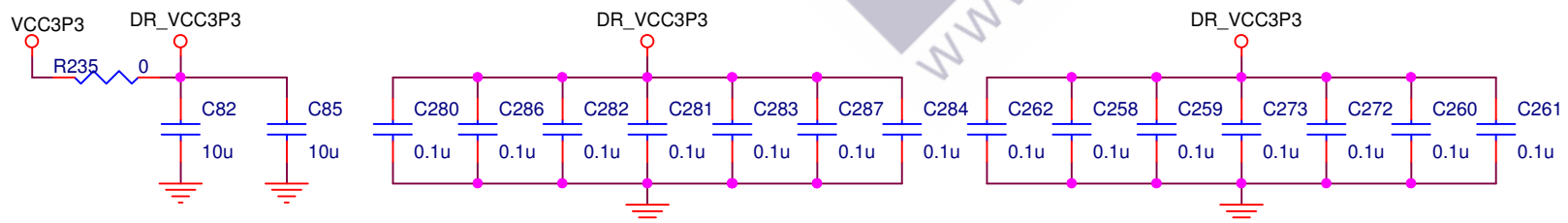
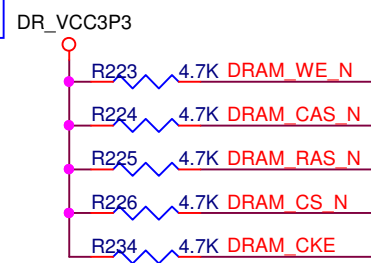
 DRAM DQ[31..0]  
 DRAM ADDR[12..0]  
 DRAM DQM[3..0]




**SDRAM0**



**SDRAM1**

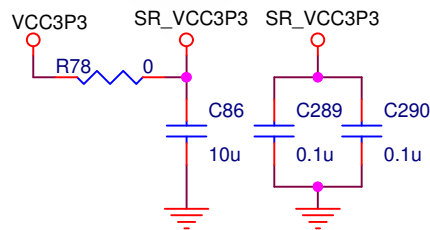
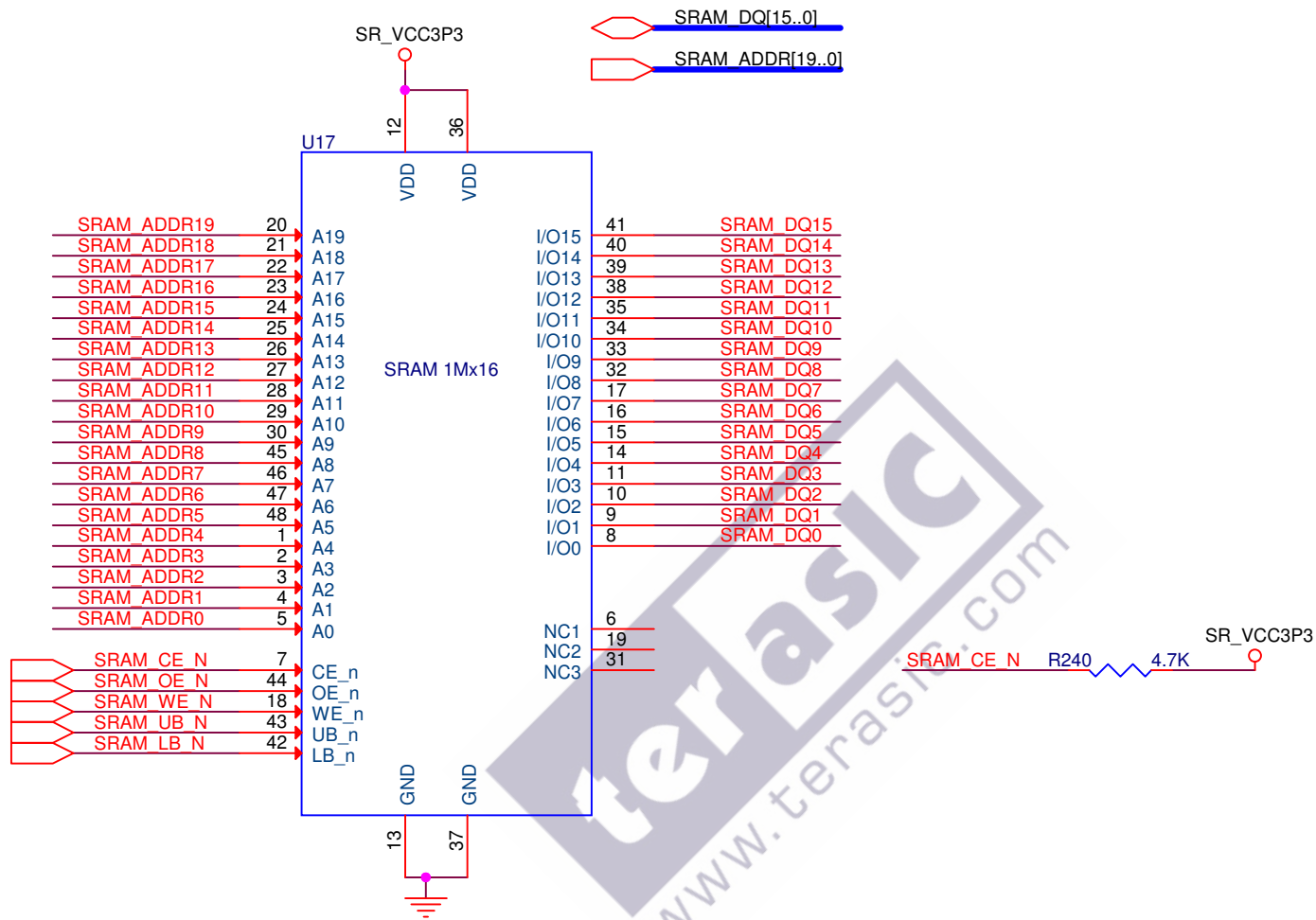



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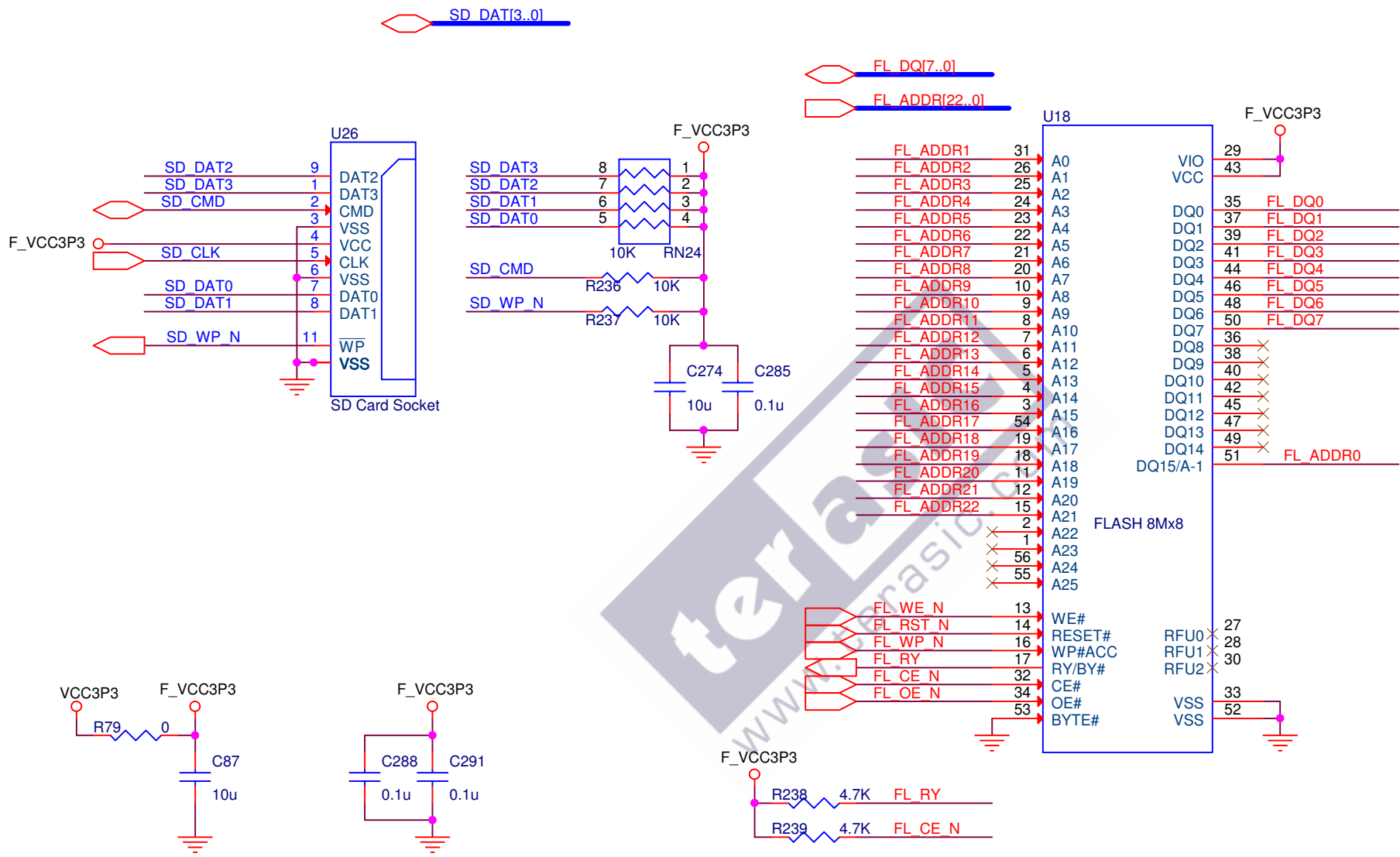
**Title**  
DE2-115 Main Board


|                  |                                 |                 |
|------------------|---------------------------------|-----------------|
| <b>Size</b><br>A | <b>Document Number</b><br>SDRAM | <b>Rev</b><br>B |
|------------------|---------------------------------|-----------------|

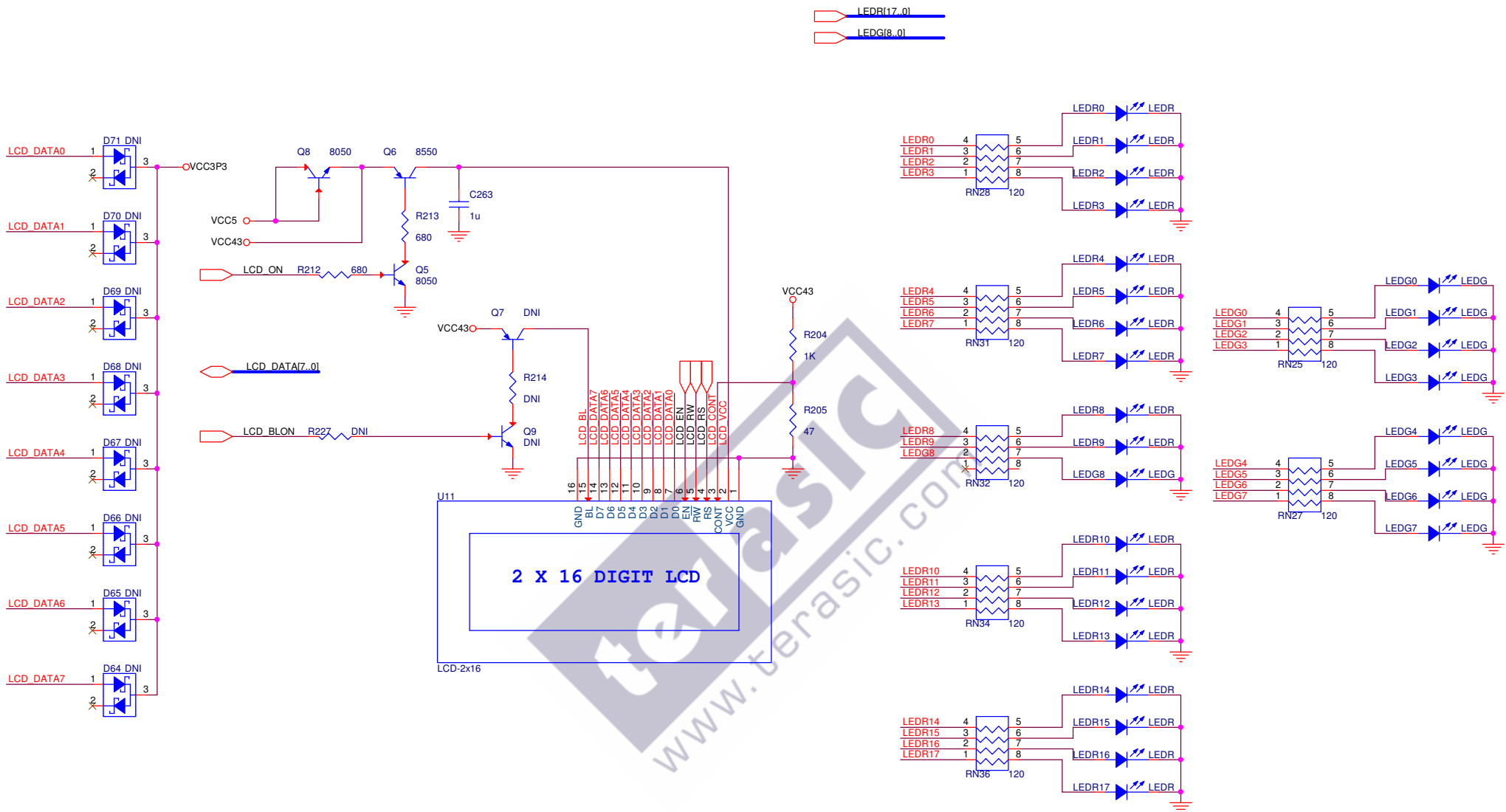
**Date:** Friday, September 24, 2010 **Sheet** 4 **of** 27



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| Title   |                            |               |
| <b>DE2-115 Main Board</b>   |                            |               |
| Size  | Document Number            | Rev           |
| A   | SRAM                       | B             |
| Date:   | Friday, September 24, 2010 | Sheet 5 of 27 |

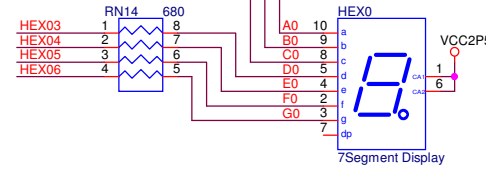
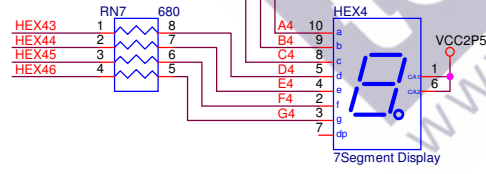
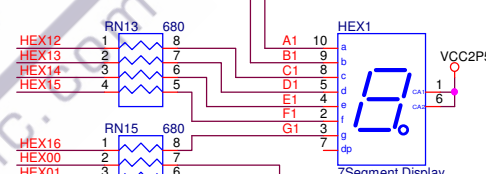
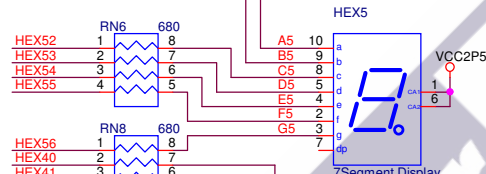
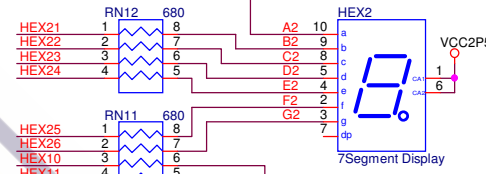
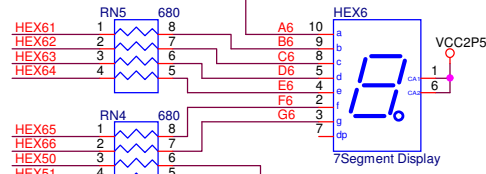
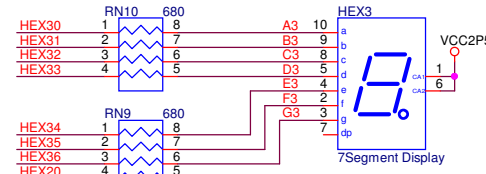
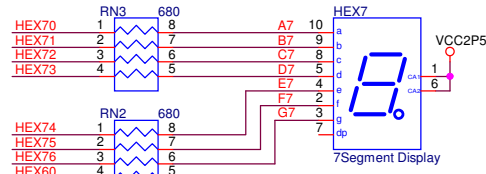


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| Title   |                            |               |
| <b>DE2-115 Main Board</b>   |                            |               |
| Size  | Document Number            | Rev           |
| A   | Flash & SD                 | B             |
| Date:   | Friday, September 24, 2010 | Sheet 6 of 27 |

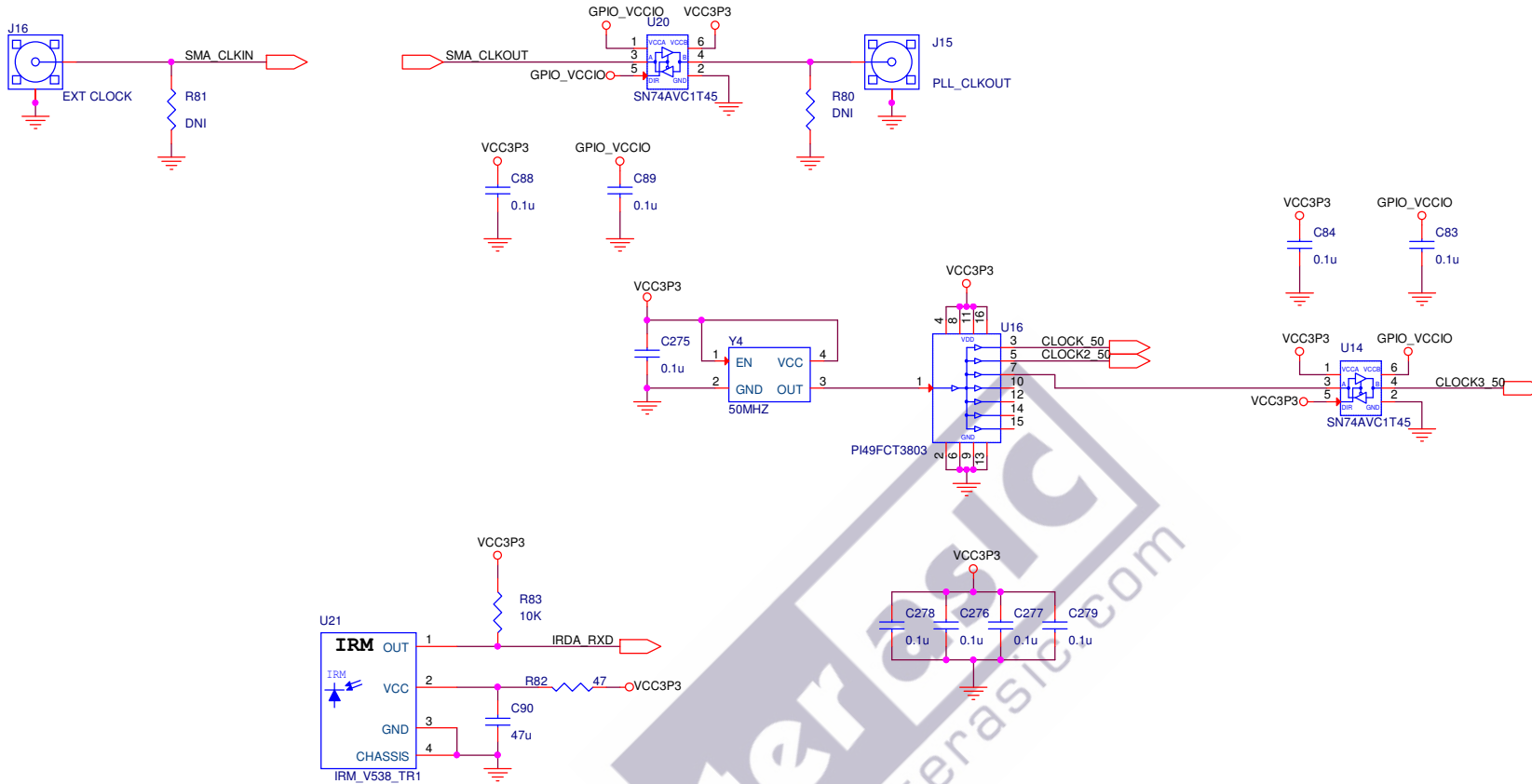



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| Title   |                            |               |
| <b>DE2-115 Main Board</b>   |                            |               |
| Size  | Document Number            | Rev           |
| B   | LCD & LED                  | B             |
| Date:   | Friday, September 24, 2010 | Sheet 7 of 27 |

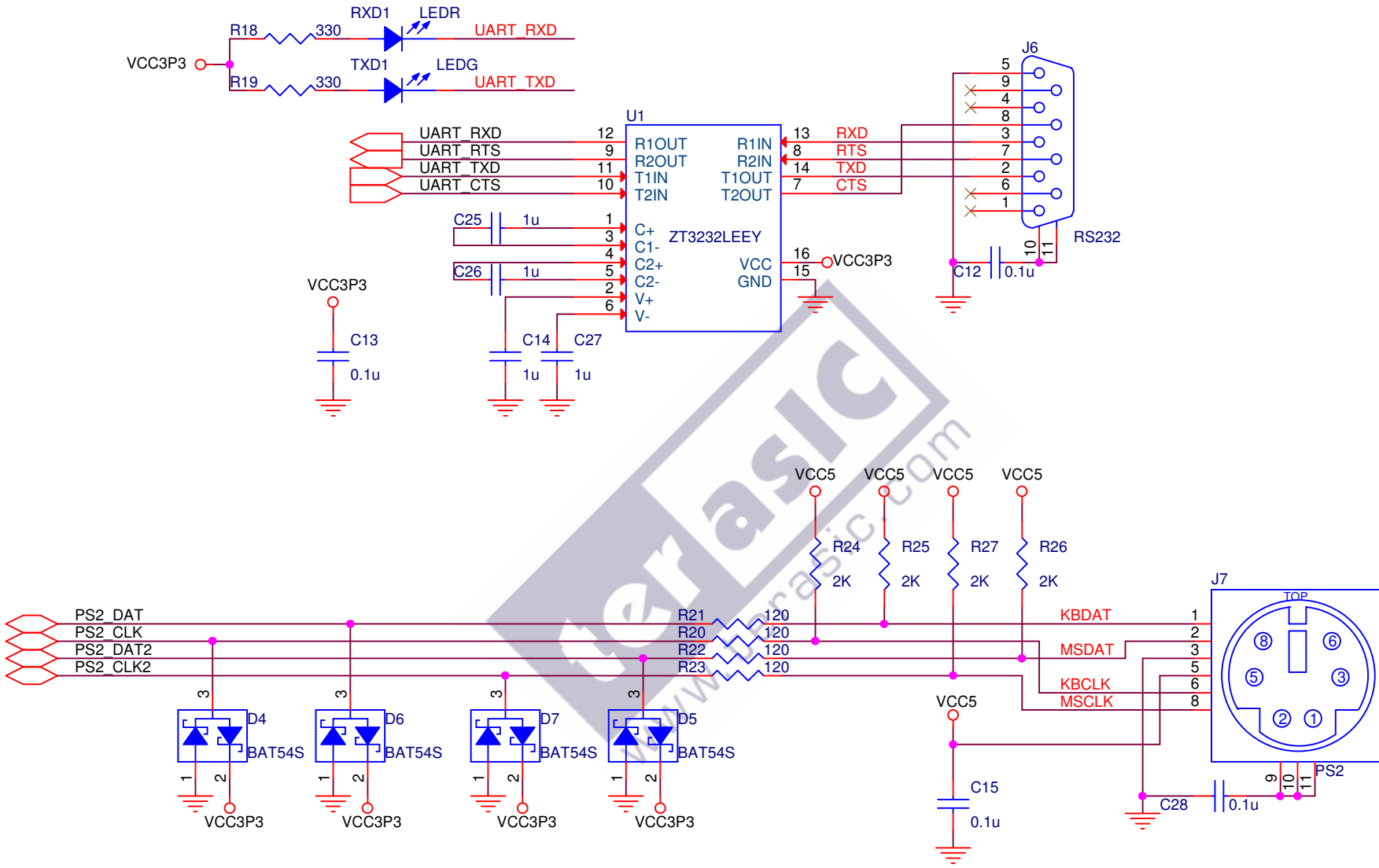
- ▶ HEX0[6..0]
- ▶ HEX1[6..0]
- ▶ HEX2[6..0]
- ▶ HEX3[6..0]
- ▶ HEX4[6..0]
- ▶ HEX5[6..0]
- ▶ HEX6[6..0]
- ▶ HEX7[6..0]




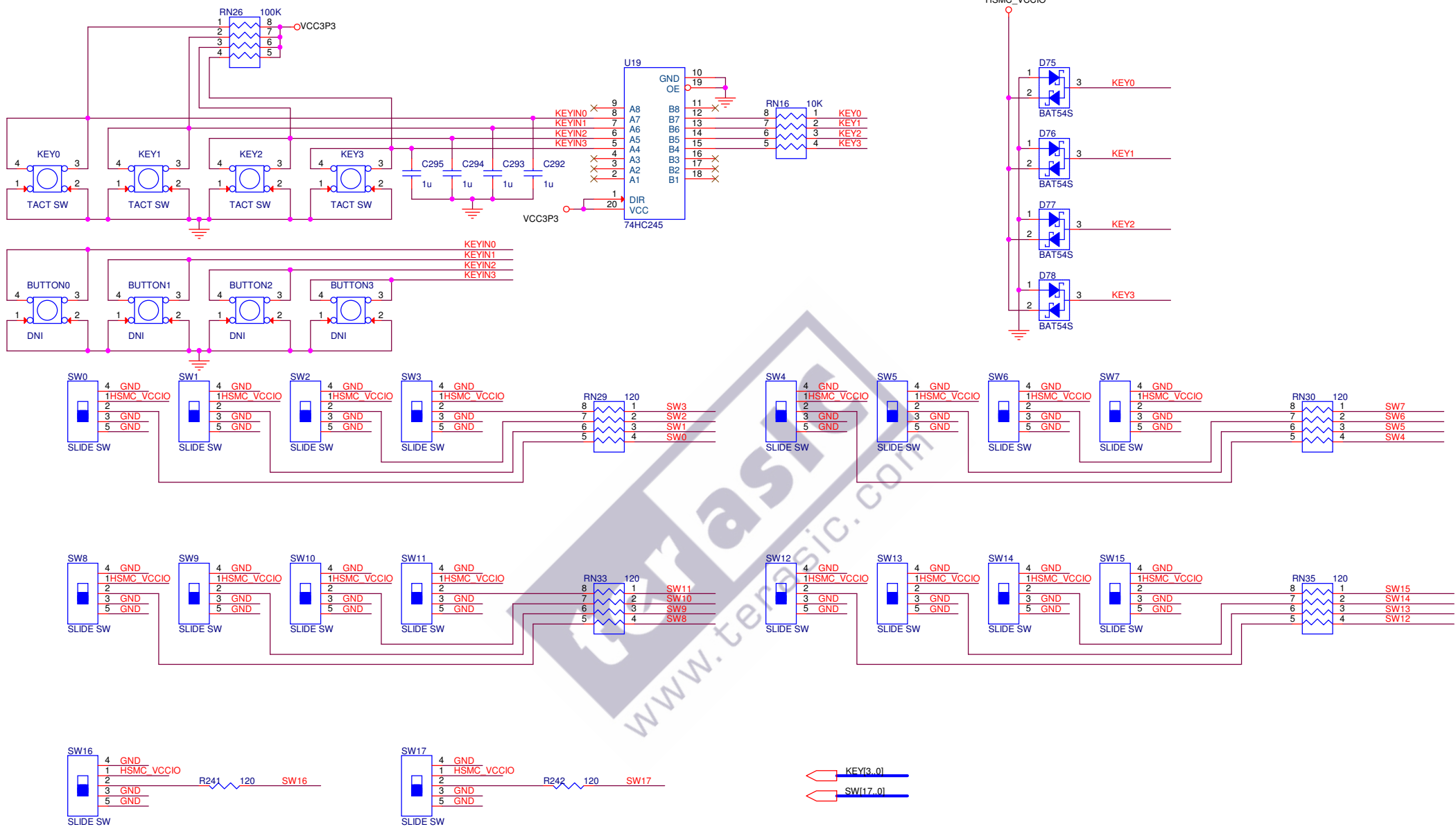




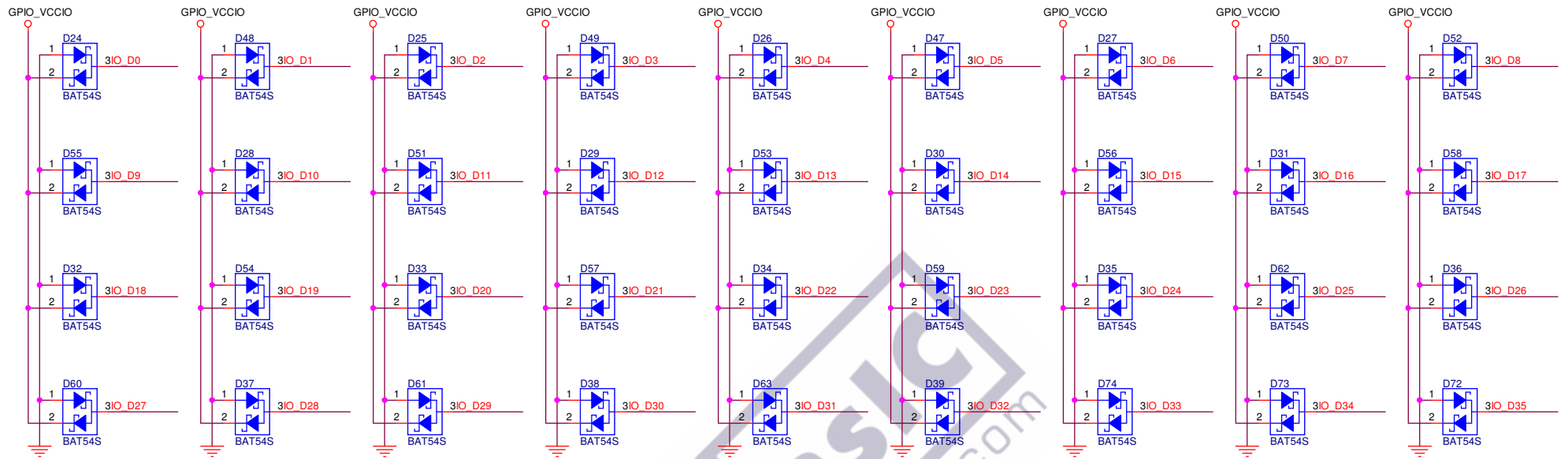
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| <b>DE2-115 Main Board</b>   |                 |
| Size  | Document Number |
| B   | CLOCK & IrDA    |
| Date:   | Rev             |
| Friday, September 24, 2010  | B               |
| Sheet   | 9 of 27         |



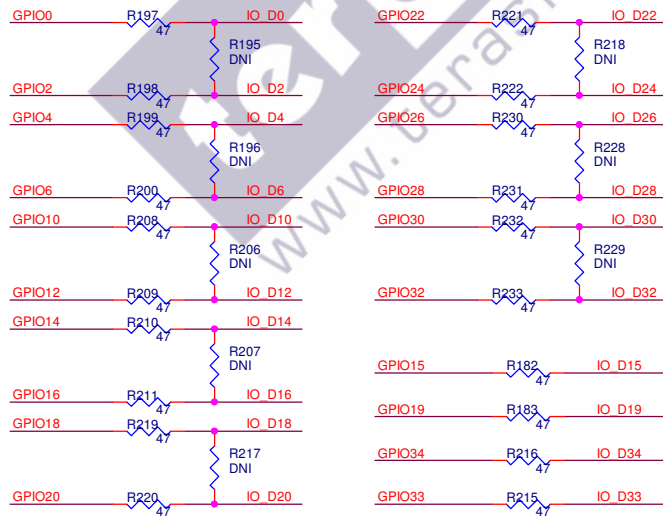
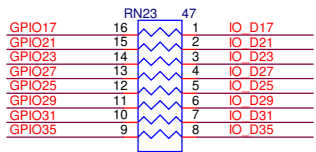
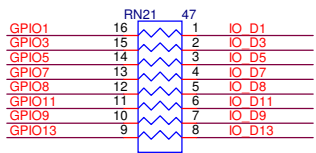
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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| A   | PS2 & RS232                | B              |
| Date:   | Friday, September 24, 2010 | Sheet 10 of 27 |



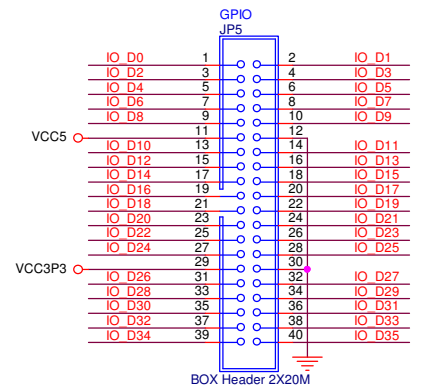
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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| B   | BUTTON & SWITCH            | B              |
| Date:   | Friday, September 24, 2010 | Sheet 11 of 27 |



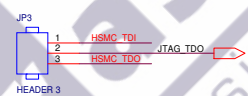
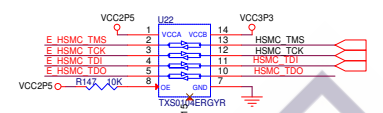
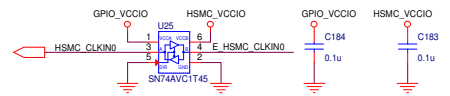
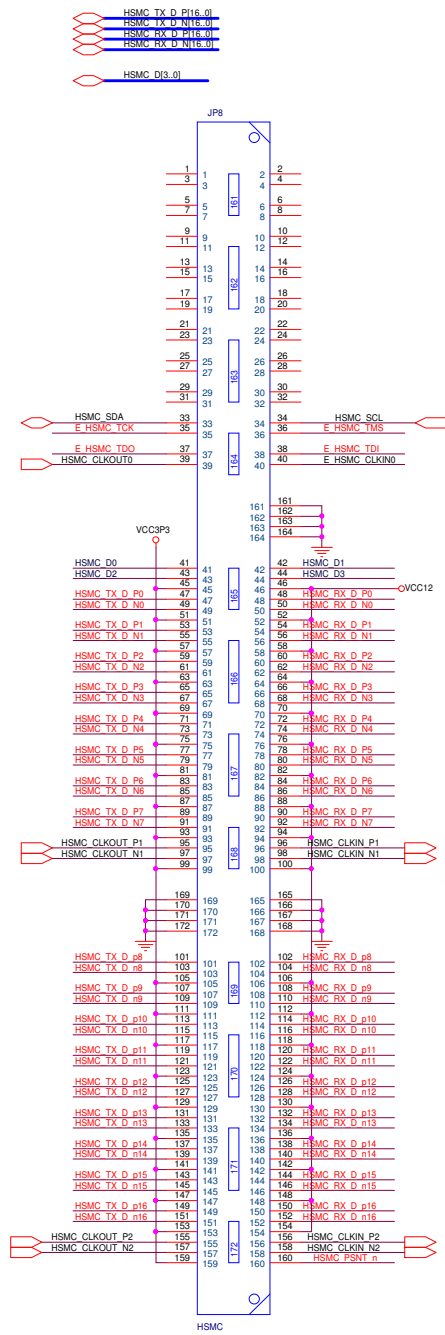
GPIOI35\_01



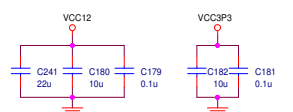
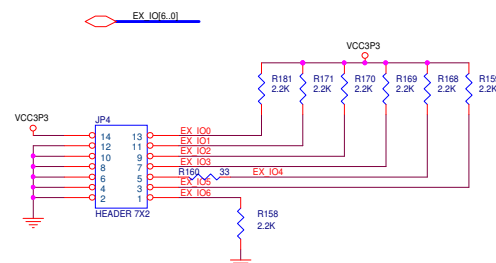
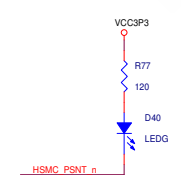
Close to FPGA

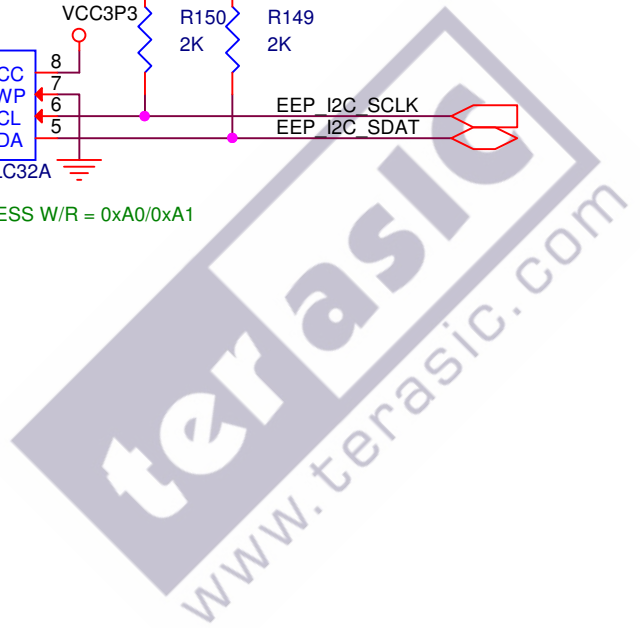
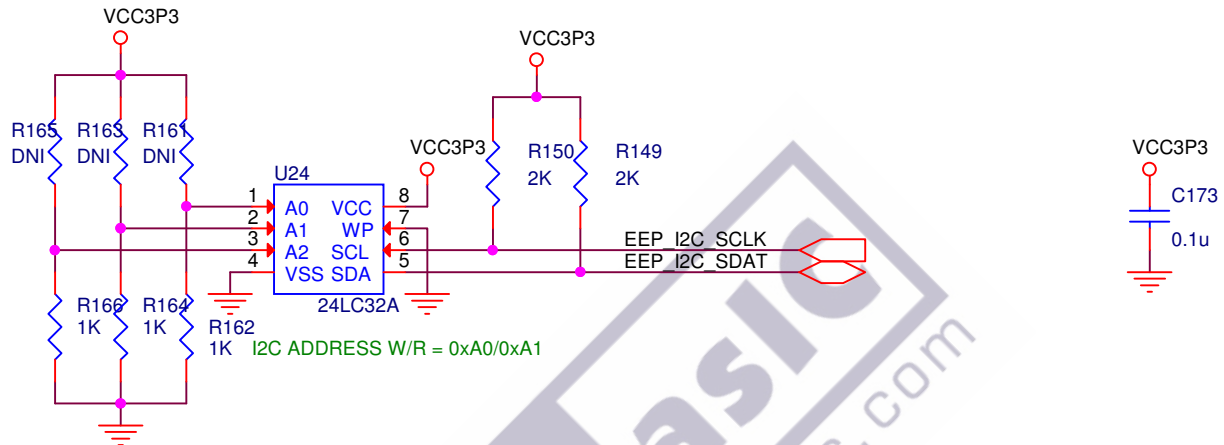



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| Title   |                            |
| <b>DE2-115 Main Board</b>   |                            |
| Size  | Document Number            |
| B   | GPIO                       |
| Date:   | Friday, September 24, 2010 |
| Sheet   | 12 of 27                   |
| Rev   | B                          |

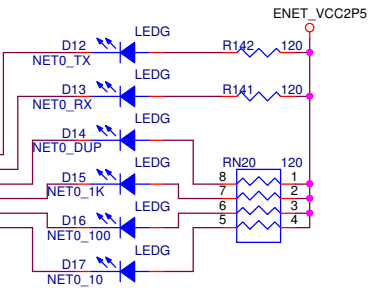
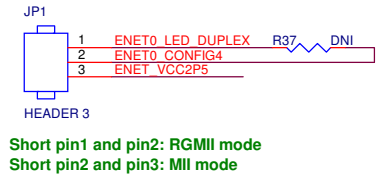
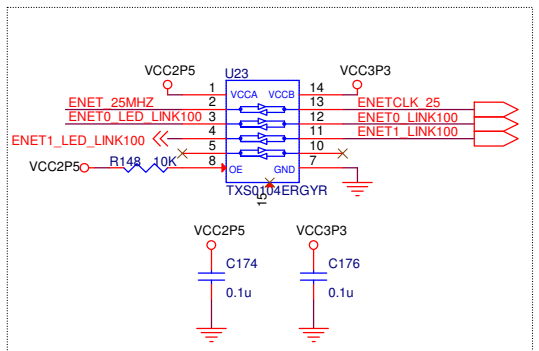
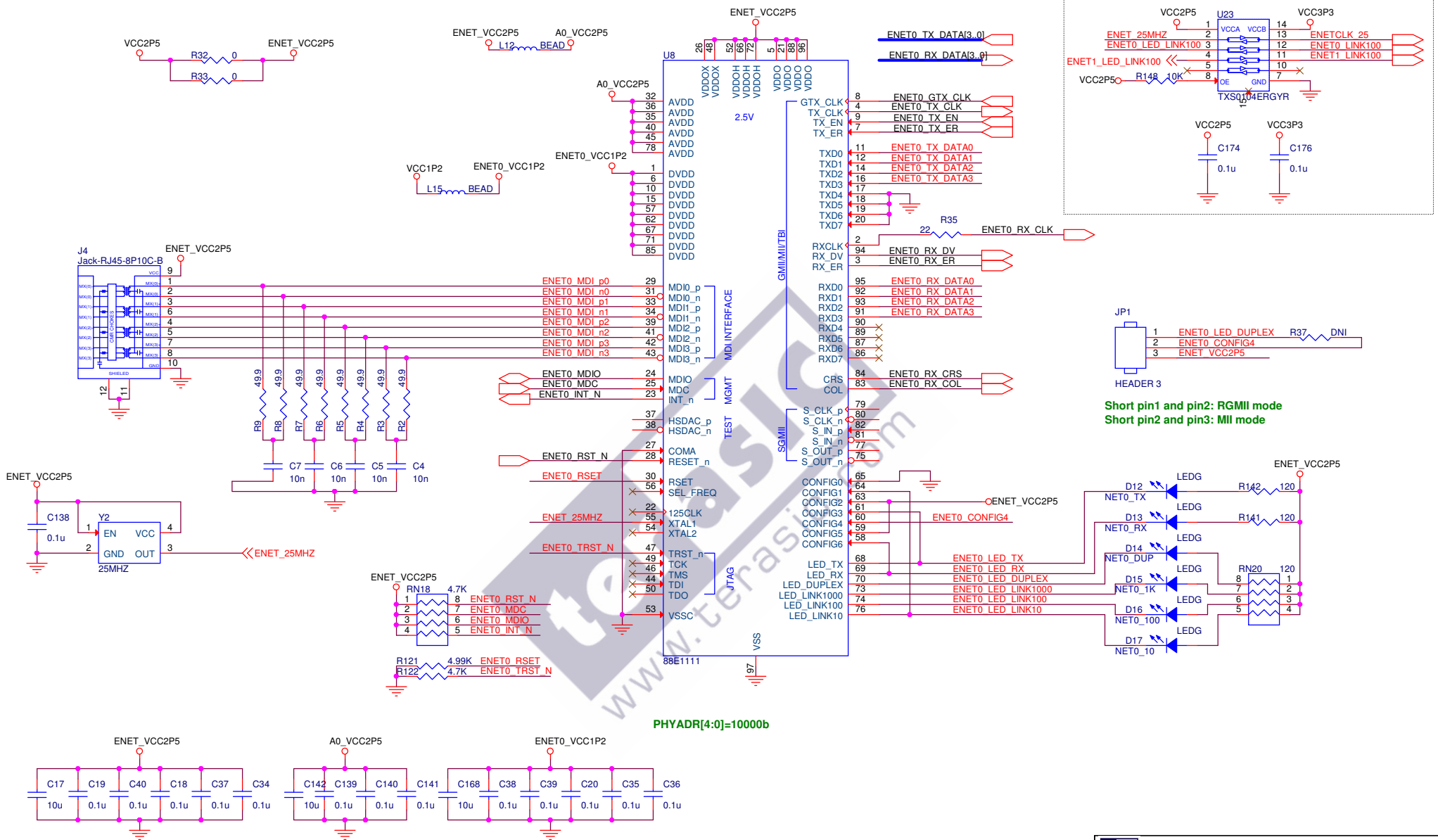


Short pin1 and pin2: JTAG chain not including HSMC  
 Short pin2 and pin3: JTAG chain including HSMC

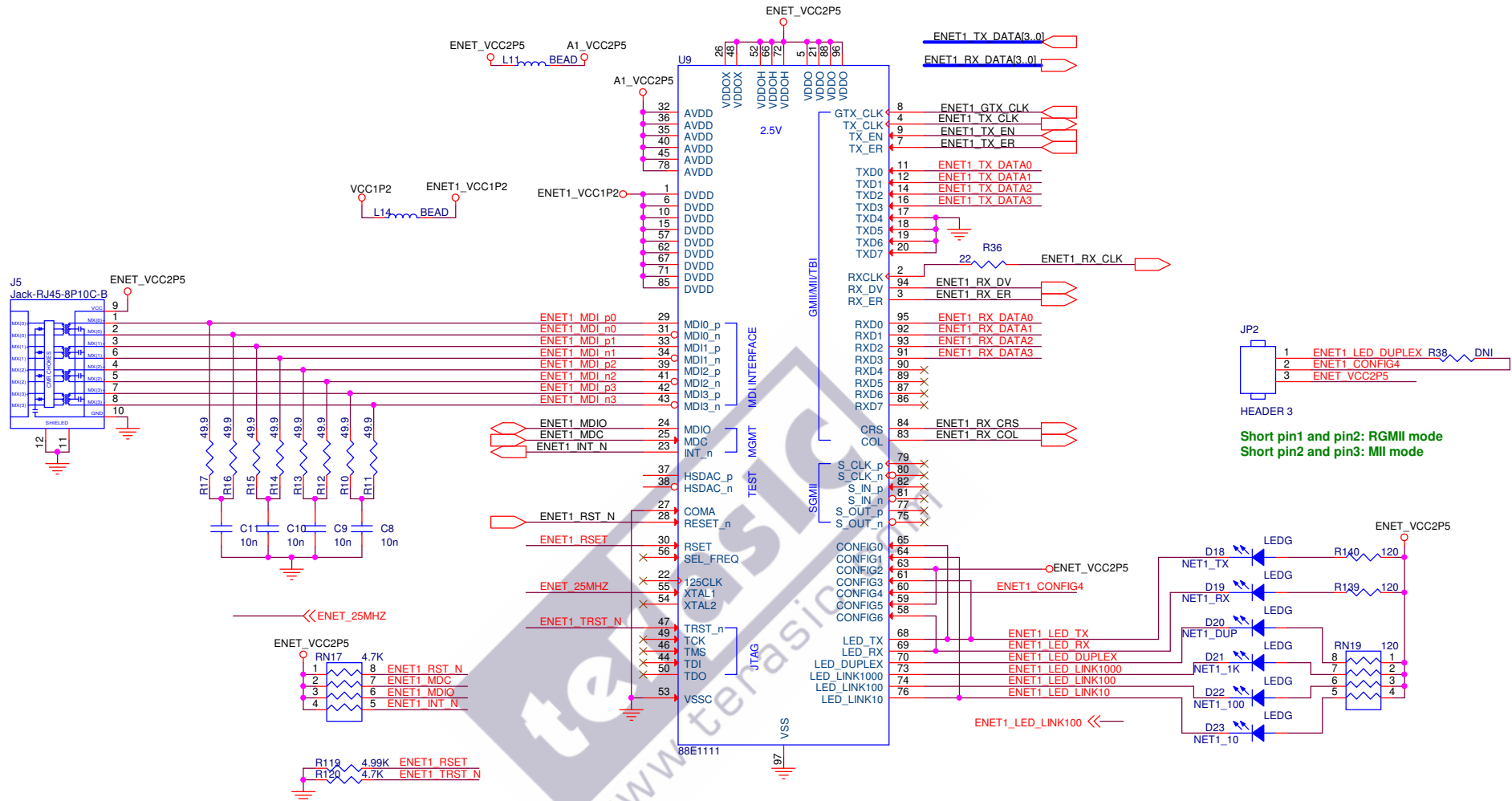




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| <b>Title</b><br><b>DE2-115 Main Board</b>   |                                  |                 |
| <b>Size</b><br>A  | <b>Document Number</b><br>EEPROM | <b>Rev</b><br>B |
| <b>Date:</b> Friday, September 24, 2010 <b>Sheet</b> 14 <b>of</b> 27  |                                  |                 |

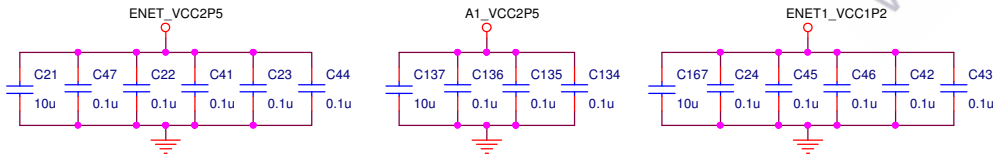


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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| B   | Ethemet 0                  | B              |
| Date:   | Friday, September 24, 2010 | Sheet 15 of 27 |



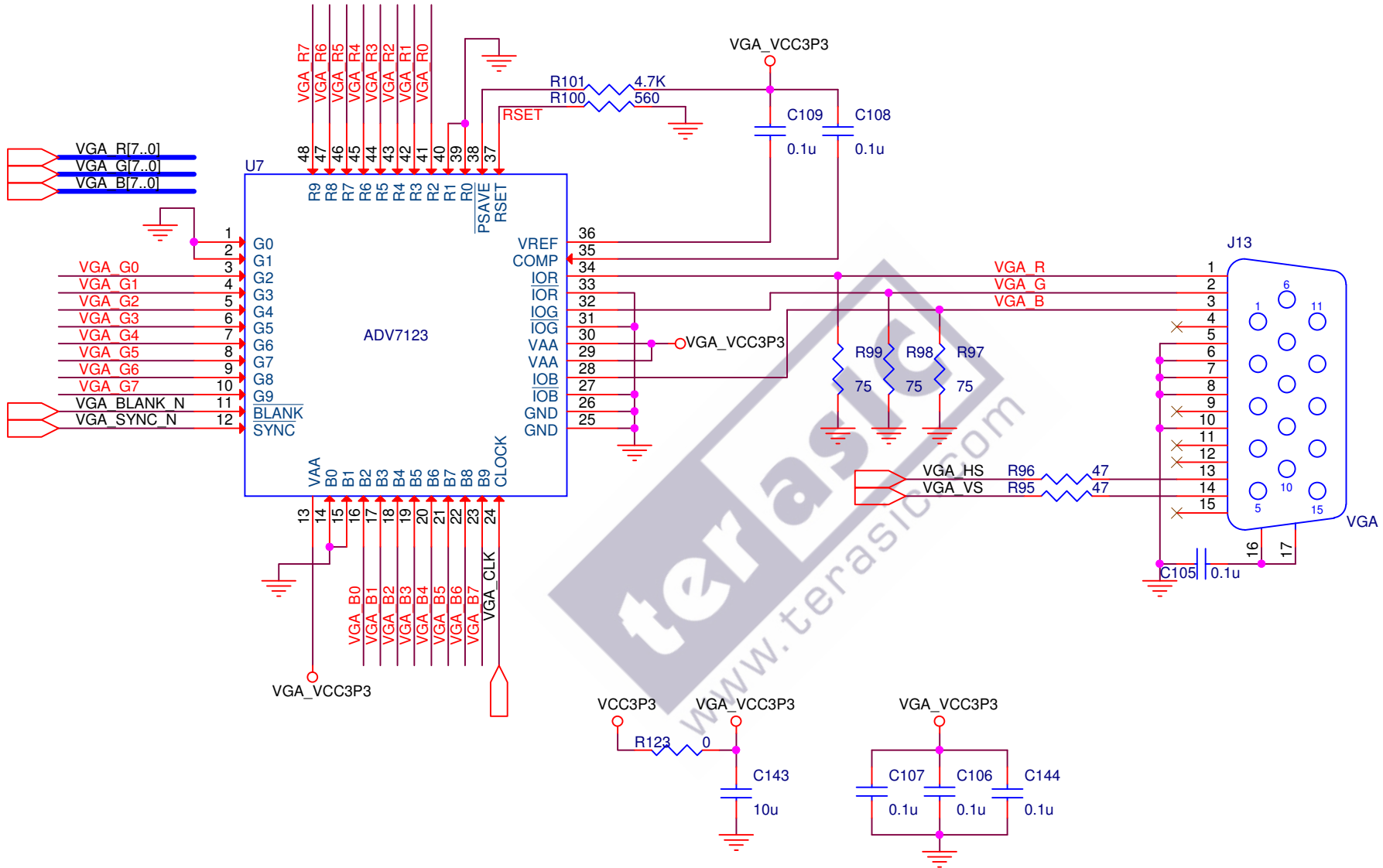
Short pin1 and pin2: RGMII mode  
Short pin2 and pin3: MII mode


PHYADR[4:0]=10001b

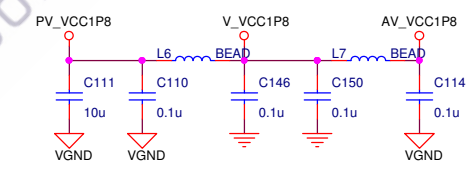
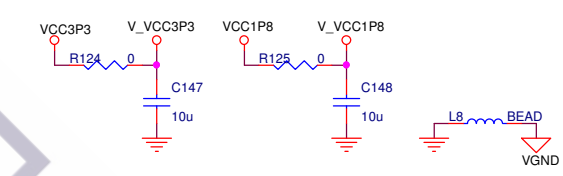
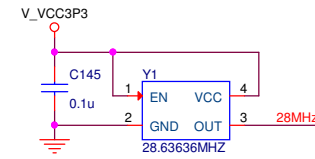
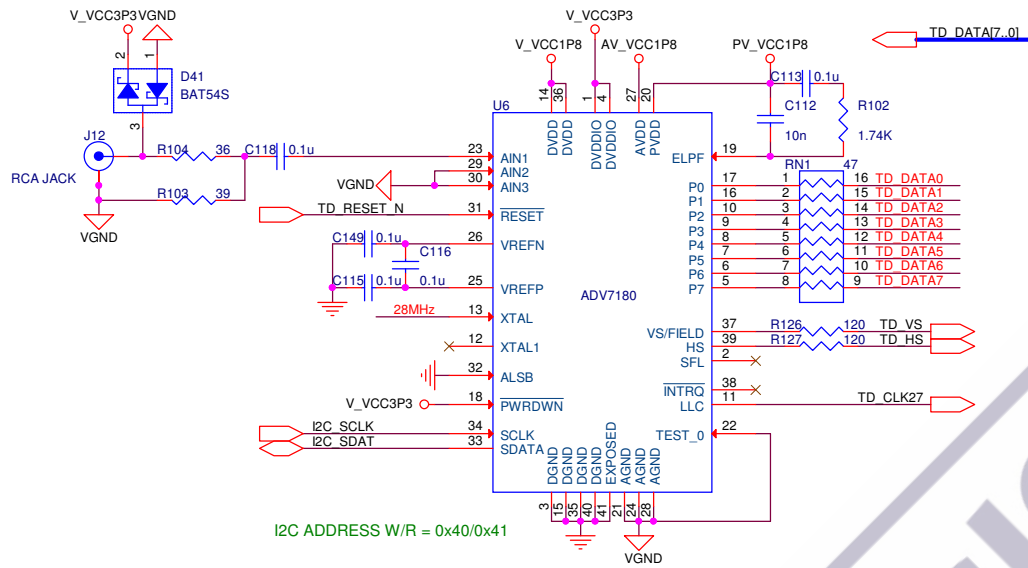


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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| B   | Ethernet 1                 | B              |
| Date:   | Friday, September 24, 2010 | Sheet 16 of 27 |

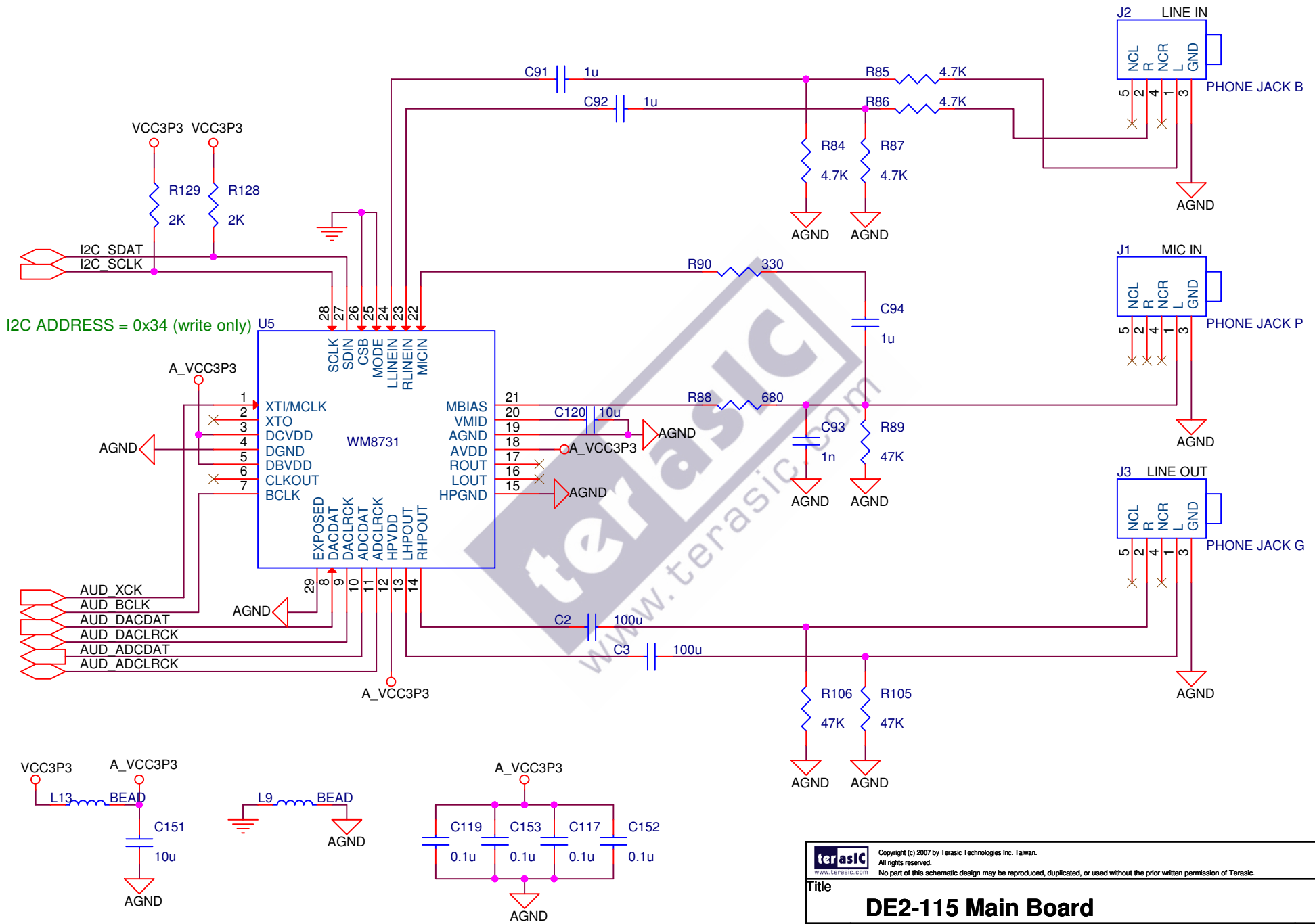





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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| A   | ADV7123 VGA                | B              |
| Date:   | Friday, September 24, 2010 | Sheet 17 of 27 |

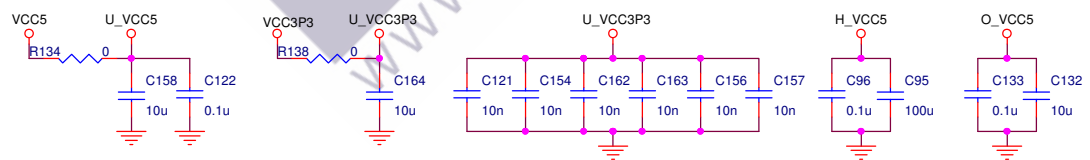
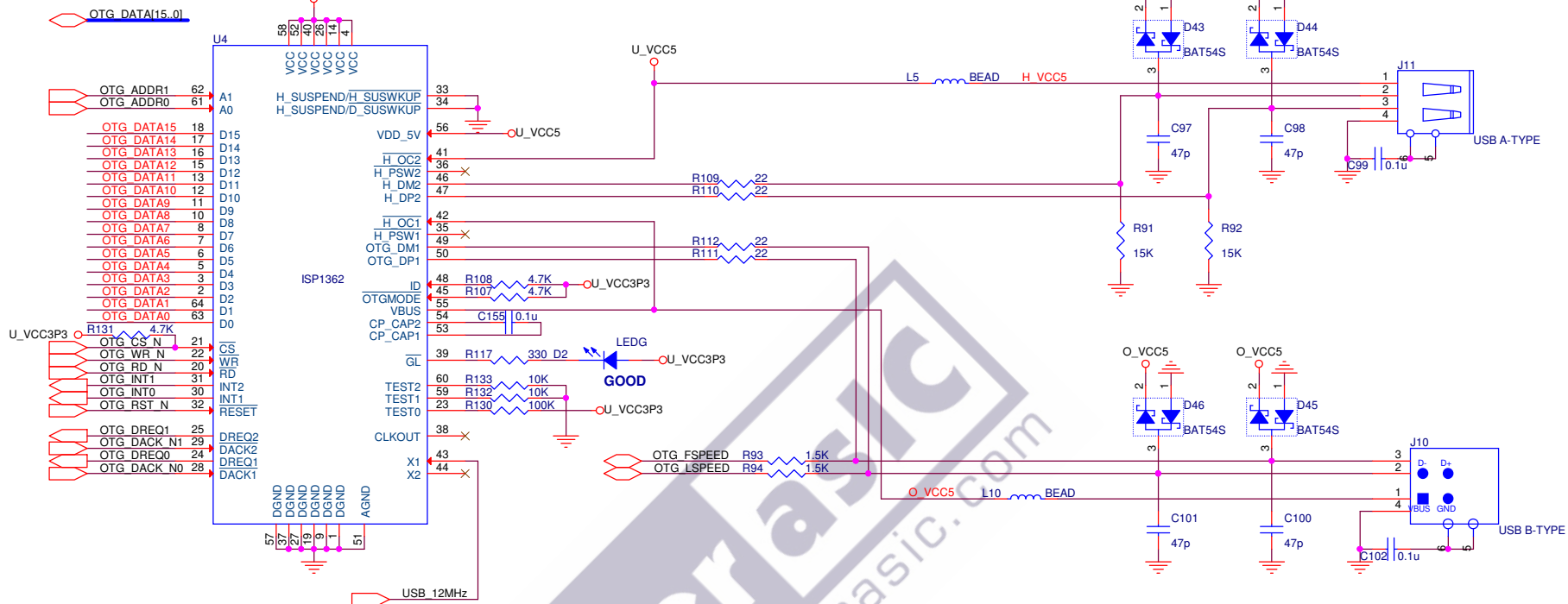


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| Title   |                 |
| <b>DE2-115 Main Board</b>   |                 |
| Size  | Document Number |
| B   | ADV7180 DECODER |
| Date:   | Rev             |
| Friday, September 24, 2010  | B               |
| Sheet   | 18 of 27        |



I2C ADDRESS = 0x34 (write only)

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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| A   | WM8731 Audio               | B              |
| Date:   | Friday, September 24, 2010 | Sheet 19 of 27 |



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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| B   | ISP1362                    | B              |
| Date:   | Friday, September 24, 2010 | Sheet 20 of 27 |

OTG\_DATA[15\_0]  
LCD\_DATA[7\_0]

DRAM\_DQ[31\_0]  
DRAM\_ADDR[12\_0]  
DRAM\_DQM[3\_0]

SRAM\_ADDR[19\_0]  
SRAM\_DQ[15\_0]

U12A  
EP4CE115F29

|             |    |                               |
|-------------|----|-------------------------------|
| AUD_ADCLRCK | C2 | DIFFIO_L1n/DQ2L               |
| AUD_ADCDAT  | D2 | DIFFIO_L2p/DQ2L               |
| AUD_DACDAT  | D1 | DIFFIO_L2n/DQ2L               |
| PS2_CLK     | G6 | DIFFIO_L2n/DQ2L               |
| PS2_CLK2    | G5 | DIFFIO_L3p/DQ2L/nRESET        |
| AUD_DACLCK  | E3 | DIFFIO_L4p/DQS2L/CQ3L/CDPCLK0 |
| OTG_DATA14  | F3 | DIFFIO_L4n/DQ2L               |
| PS2_DAT2    | F5 | DIFFIO_L5p/DQ2L               |
| OTG_DATA15  | G4 | DIFFIO_L6p/DQ2L               |
| OTG_DATA12  | G3 | DIFFIO_L6n                    |
| OTG_DATA9   | H4 | DIFFIO_L7p                    |
| OTG_DATA8   | H3 | DIFFIO_L7n                    |
| AUD_XCK     | E1 | DIFFIO_L8n                    |
| AUD_BCLK    | F2 | DIFFIO_L9p/DM2L               |
| OTG_DATA13  | F1 | DIFFIO_L9n/DQ0L               |
| OTG_DATA4   | J4 | DIFFIO_L10p                   |
| OTG_DATA5   | J3 | DIFFIO_L10n/DQ0L              |
| OTG_DATA11  | G2 | DIFFIO_L11p/DQ0L              |
| OTG_DATA10  | G1 | DIFFIO_L11n                   |
| LCD_DATA5   | K2 | DIFFIO_L12p/DQS0L/CQ1L/DPCLK0 |
| LCD_DATA4   | K1 | DIFFIO_L12n/DQ0L              |
| OTG_DATA1   | K4 | DIFFIO_L13p                   |
| OTG_DATA3   | K3 | DIFFIO_L13n                   |
| LCD_EN      | L4 | DIFFIO_L14p                   |
| LCD_DATA0   | L3 | DIFFIO_L14n                   |
| DRAM_DQ21   | M4 | DIFFIO_L15p                   |
| LCD_DATA6   | M3 | DIFFIO_L15n                   |
| OTG_DATA0   | J6 | DIFFIO_L18p                   |
| OTG_DATA2   | J5 | DIFFIO_L16n                   |
| OTG_DATA6   | J7 | DIFFIO_L17p                   |
| LCD_DATA3   | K7 | DIFFIO_L17n                   |
| DRAM_DQM2   | K8 | DIFFIO_L18p                   |
| DRAM_DQ17   | L8 | DIFFIO_L18n                   |
| DRAM_DQ23   | L7 | DIFFIO_L19p                   |
| LCD_BLON    | L6 | DIFFIO_L19n                   |
| DRAM_DQ20   | N4 | DIFFIO_L20p                   |
| DRAM_DQ19   | N3 | DIFFIO_L20n                   |
| DRAM_DQ16   | M8 | DIFFIO_L21p                   |
| DRAM_DQ22   | M7 | DIFFIO_L21n                   |
| LCD_DATA2   | L2 | DIFFIO_L22p                   |
| LCD_DATA1   | L1 | DIFFIO_L22n/DQ0L              |
| LCD_RS      | M1 | DIFFIO_L23p                   |
| LCD_RW      | M1 | DIFFIO_L23n/DQ0L              |
| DRAM_DQ18   | P2 | DIFFIO_L24p                   |
| DRAM_ADDR3  | P1 | DIFFIO_L24n/DQ0L              |

BANK1

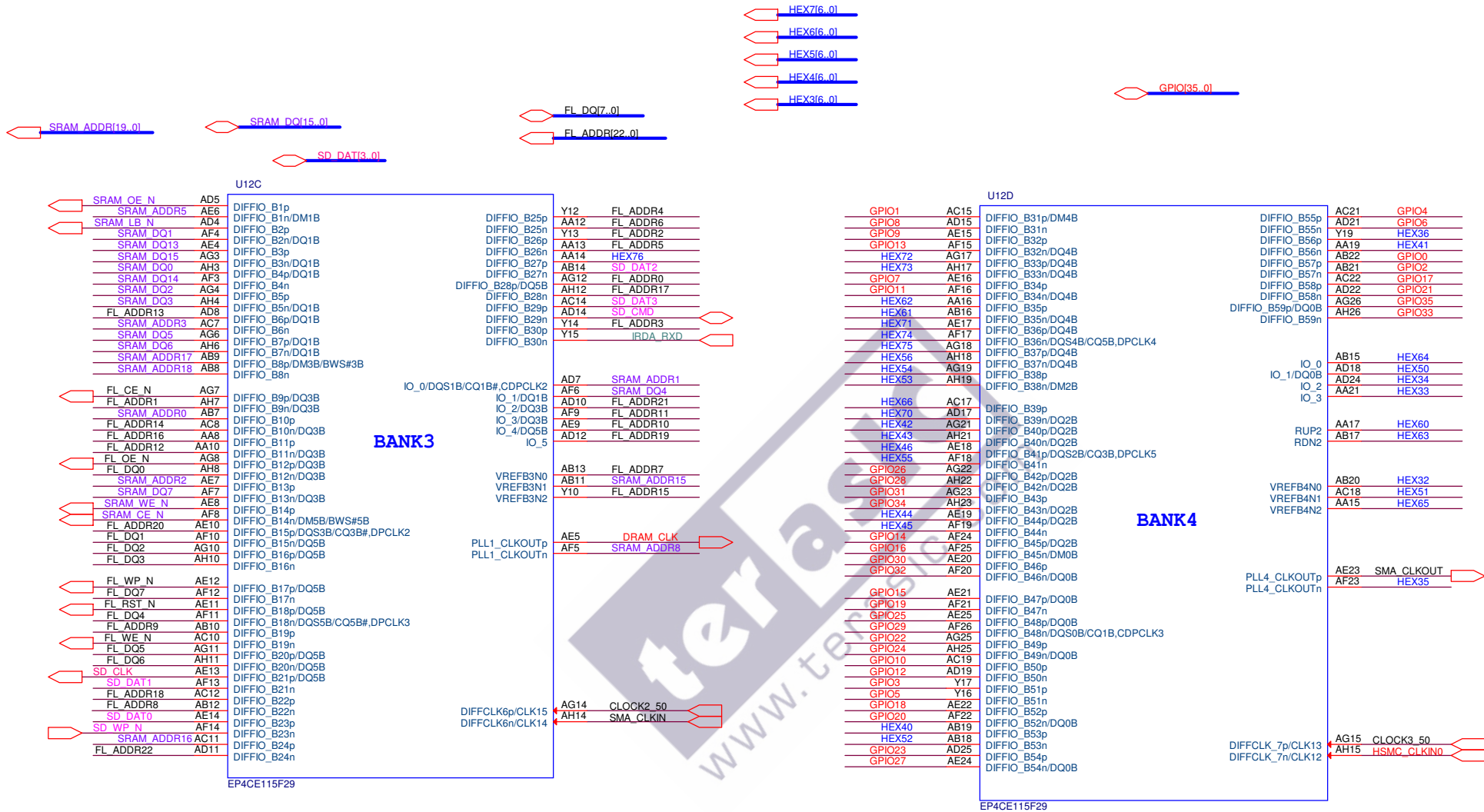
H6 OTG\_DATA7  
H5 PS2\_DAT  
N8 DRAM\_DQM3  
H7 OTG\_ADDR0  
L5 LCD\_ON  
M5 LCD\_DATA7  
VREFB1N0  
VREFB1N1  
VREFB1N2  
DIFFCLK\_0n/CLK1  
J1 OTG\_DREQ0

U12B  
EP4CE115F29

|             |     |                                 |
|-------------|-----|---------------------------------|
| DRAM_DQ27   | R2  | DIFFIO_L25p/DQ0L                |
| DRAM_DQ26   | R1  | DIFFIO_L25n                     |
| DRAM_DQ25   | R7  | DIFFIO_L26p                     |
| DRAM_ADDR0  | R6  | DIFFIO_L26n                     |
| DRAM_DQ7    | U3  | DIFFIO_L27p/DM0L                |
| DRAM_DQ30   | U4  | DIFFIO_L27n                     |
| DRAM_DQ28   | R3  | DIFFIO_L28p/DQ1L                |
| DRAM_BA1    | R4  | DIFFIO_L28n/DQ1L                |
| DRAM_CS_N   | T4  | DIFFIO_L29p/DQ1L                |
| DRAM_DQ29   | T3  | DIFFIO_L29n                     |
| DRAM_DQM0   | U2  | DIFFIO_L30p                     |
| DRAM_DQ31   | U1  | DIFFIO_L30n/DQ1L                |
| DRAM_DQ2    | V4  | DIFFIO_L31p/DQ1L                |
| DRAM_DQ4    | V3  | DIFFIO_L31n                     |
| DRAM_DQ5    | V2  | DIFFIO_L32p/DQ1L                |
| DRAM_DQ6    | V1  | DIFFIO_L32n/DQ1L                |
| DRAM_DQ12   | AB2 | DIFFIO_L33p/DQS1L/CQ1L#/DPCLK1  |
| DRAM_DQ10   | AB1 | DIFFIO_L33n                     |
| DRAM_DQ1    | W2  | DIFFIO_L34p/DQ1L                |
| DRAM_DQ3    | W1  | DIFFIO_L34n/DM1L/BWS#1L         |
| DRAM_RAS_N  | U6  | DIFFIO_L35p/DQ3L                |
| DRAM_DQ24   | U5  | DIFFIO_L35n                     |
| DRAM_DQ8    | Y4  | DIFFIO_L36p/DQ3L                |
| DRAM_DQ8    | Y3  | DIFFIO_L36n                     |
| DRAM_DQ15   | AC2 | DIFFIO_L37p/DQ3L                |
| DRAM_DQ13   | AC1 | DIFFIO_L37n/DQ3L                |
| SRAM_ADDR13 | AC3 | DIFFIO_L38p/DQ3L                |
| SRAM_ADDR11 | AD3 | DIFFIO_L38n                     |
| SRAM_DQ9    | AD2 | DIFFIO_L39p/DQ3L                |
| SRAM_DQ8    | AD1 | DIFFIO_L39n                     |
| SRAM_ADDR14 | AA4 | DIFFIO_L40p/DQ3L                |
| DRAM_DQ11   | AA3 | DIFFIO_L40n                     |
| SRAM_DQ10   | AE2 | DIFFIO_L41p/DQ3L                |
| SRAM_DQ11   | AE1 | DIFFIO_L41n                     |
| DRAM_WE_N   | V6  | DIFFIO_L42p                     |
| DRAM_ADDR4  | V5  | DIFFIO_L42n                     |
| DRAM_ADDR1  | V8  | DIFFIO_L43P                     |
| DRAM_CAS_N  | V7  | DIFFIO_L43n                     |
| DRAM_DQM1   | W4  | DIFFIO_L44p                     |
| DRAM_DQ0    | W3  | DIFFIO_L44n                     |
| DRAM_ADDR9  | Y6  | DIFFIO_L45p                     |
| DRAM_ADDR8  | Y5  | DIFFIO_L45n                     |
| DRAM_ADDR5  | W8  | DIFFIO_L46p                     |
| DRAM_ADDR12 | Y7  | DIFFIO_L46n                     |
| DRAM_CKE    | AA6 | DIFFIO_L47p                     |
| DRAM_ADDR11 | AA5 | DIFFIO_L47n                     |
| SRAM_DQ12   | AE3 | DIFFIO_L48p/DQS3L/CQ3L#/CDPCLK1 |
| SRAM_ADDR10 | AF2 | DIFFIO_L48n/DM3L/BWS#3L         |
| SRAM_ADDR7  | AC5 | DIFFIO_L49p                     |
| SRAM_UB_N   | AC4 | DIFFIO_L49n                     |
| SRAM_ADDR4  | AB6 | DIFFIO_L50p                     |
| SRAM_ADDR6  | AB5 | DIFFIO_L50n                     |

BANK2

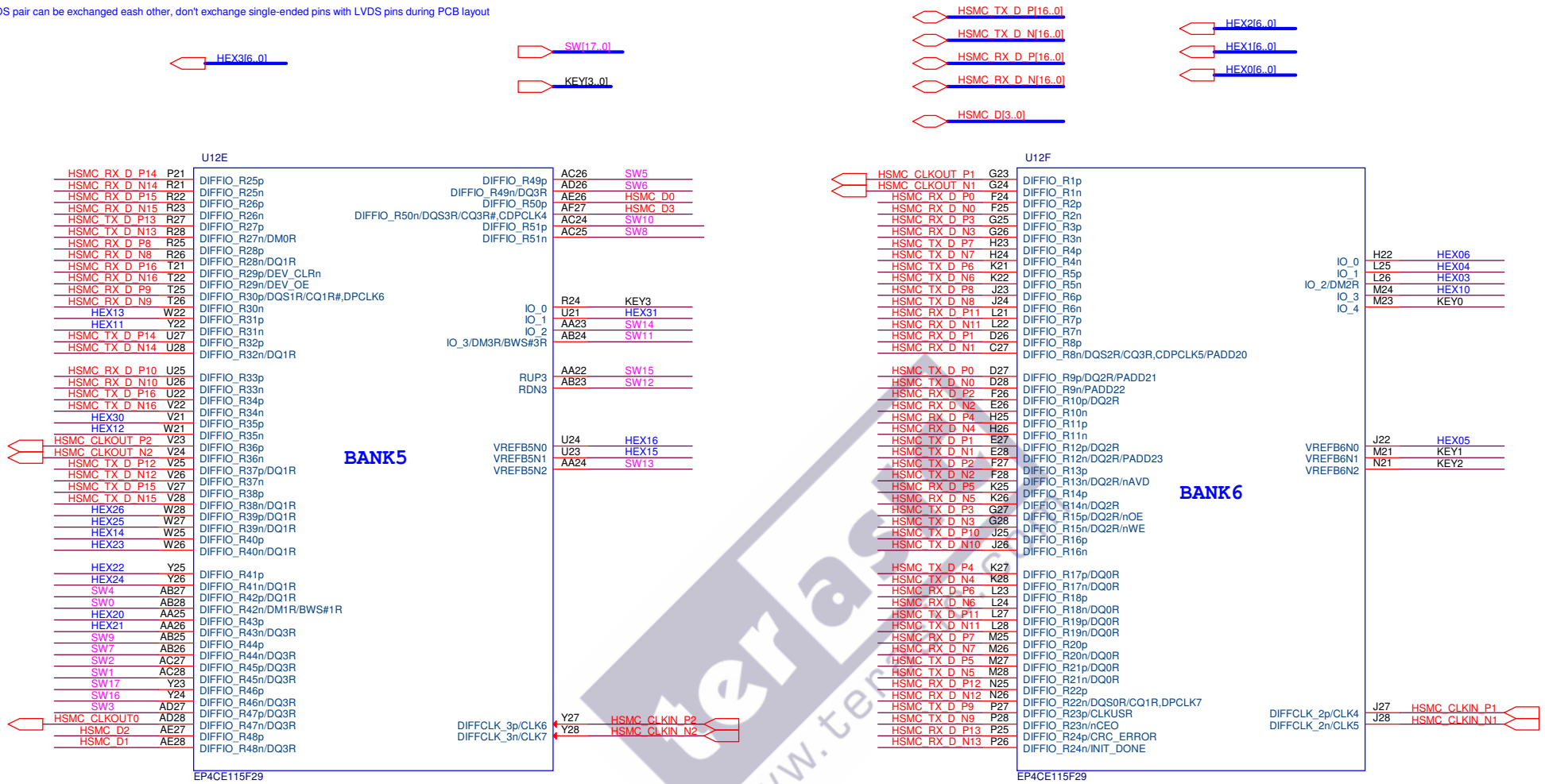
R5 DRAM\_ADDR10  
AB3 DRAM\_DQ14  
W7 DRAM\_ADDR6  
AA7 DRAM\_ADDR7  
IO\_0/DQ1L  
IO\_1/DQ3L  
IO\_2  
IO\_3  
U7 DRAM\_BA0  
U8 DRAM\_ADDR2  
RUP1  
RDN1  
VREFB2N0  
VREFB2N1  
VREFB2N2  
T7 SRAM\_ADDR9  
T8 SRAM\_ADDR19  
AB4 SRAM\_ADDR12  
DIFFCLK\_1p/CLK2  
DIFFCLK\_1n/CLK3  
Y2 CLOCK\_50  
Y1 FL\_RY



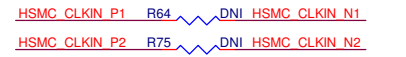
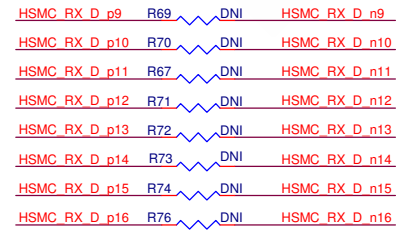
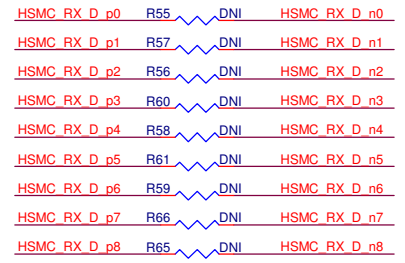
The LVDS pair can be exchanged each other, don't exchange single-ended pins with LVDS pins during PCB layout

|   |                            |                |
|---|----------------------------|----------------|
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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| B   | EP4CE115 BANK 3 and BANK 4 | B              |
| Date:   | Friday, September 24, 2010 | Sheet 22 of 27 |

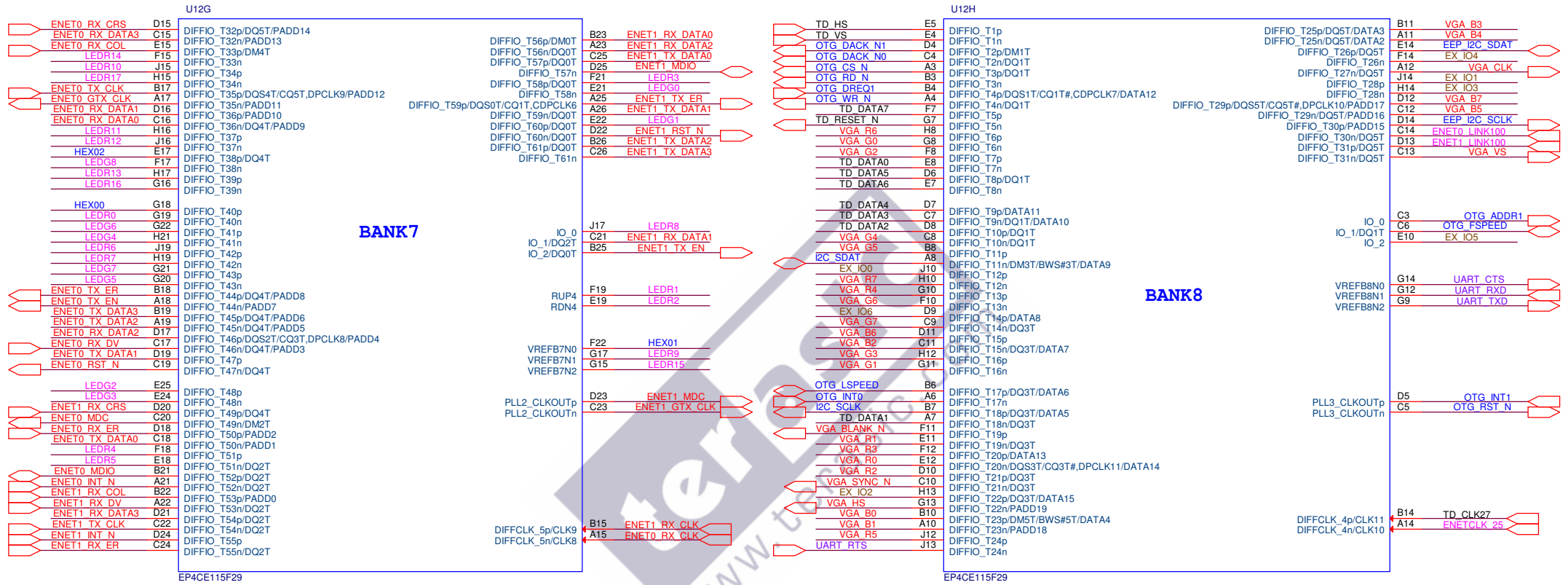
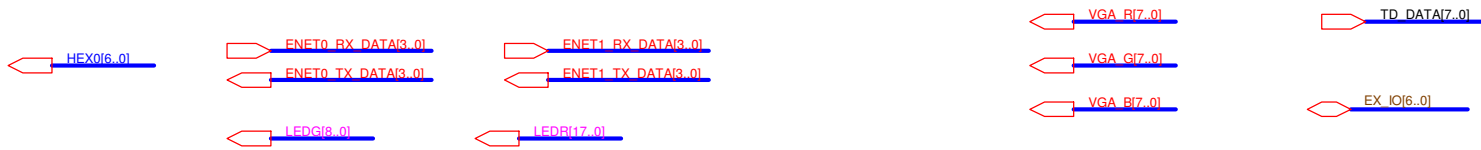
The LVDS pair can be exchanged each other, don't exchange single-ended pins with LVDS pins during PCB layout



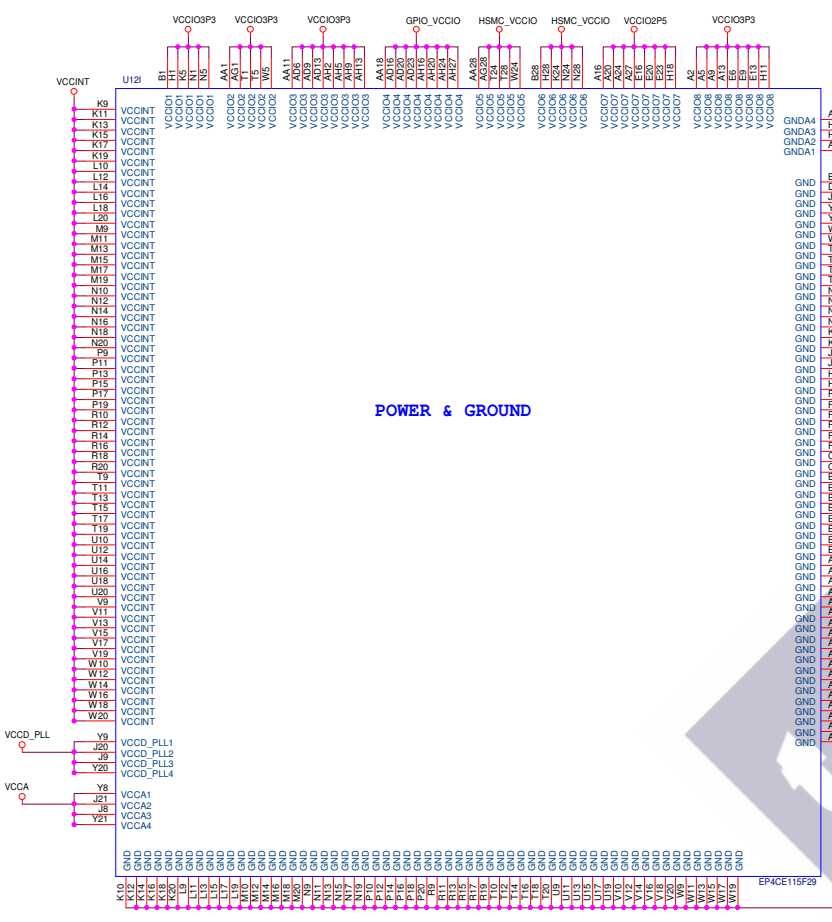
Close to FPGA



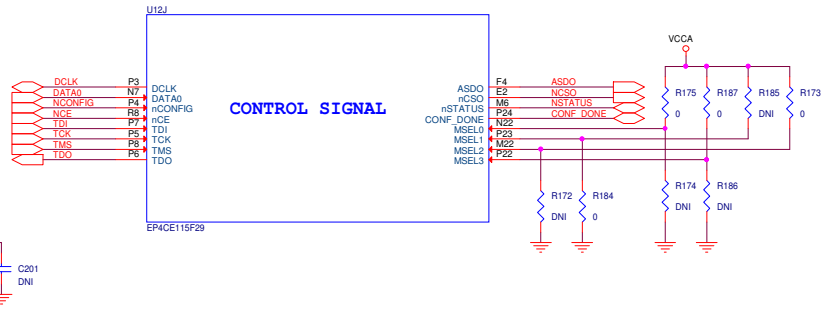
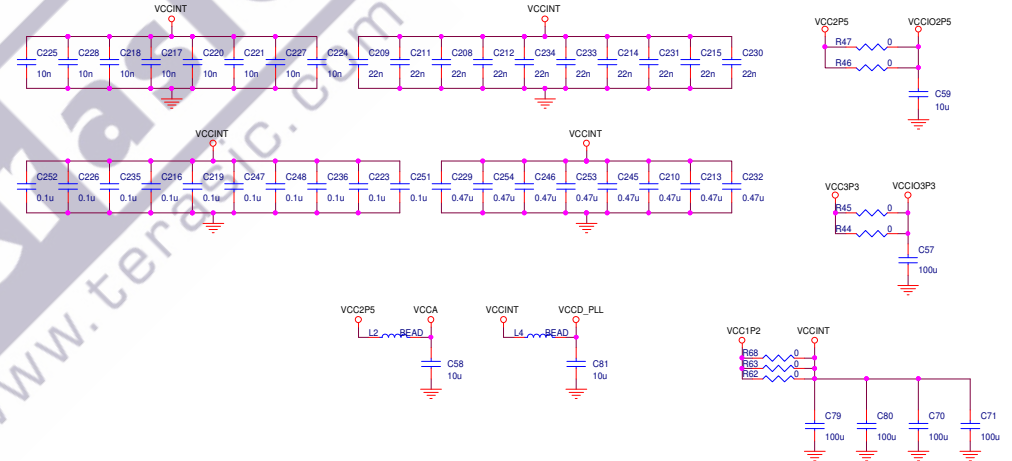
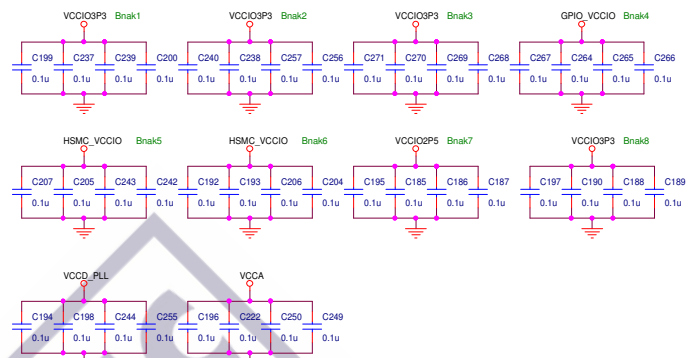
|   |                            |                |
|---|----------------------------|----------------|
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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| B   | EP4CE115 BANK 5 and BANK 6 | B              |
| Date:   | Friday, September 24, 2010 | Sheet 23 of 27 |

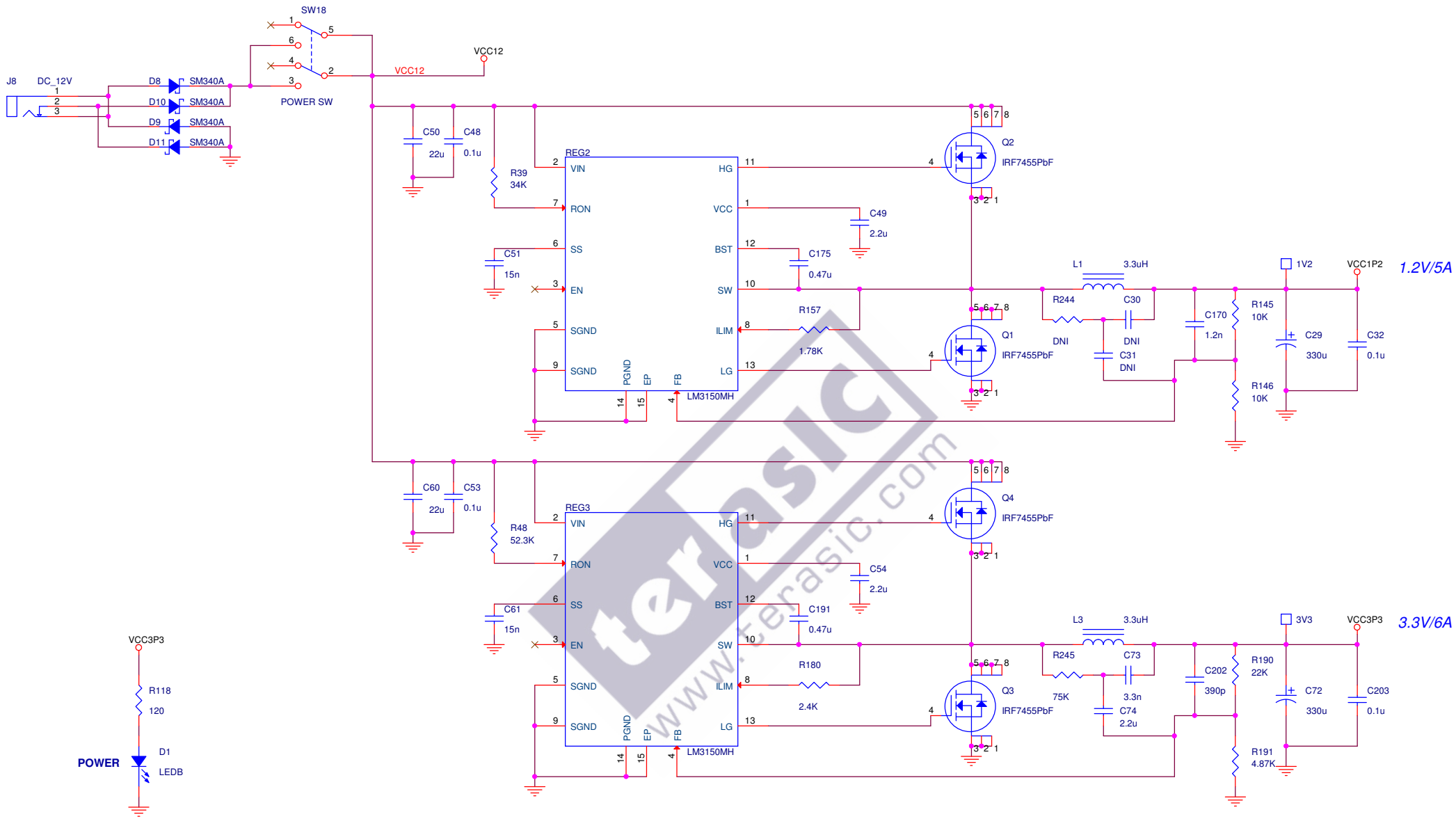





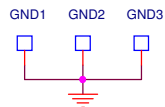
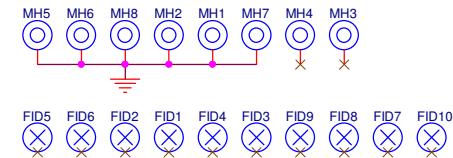
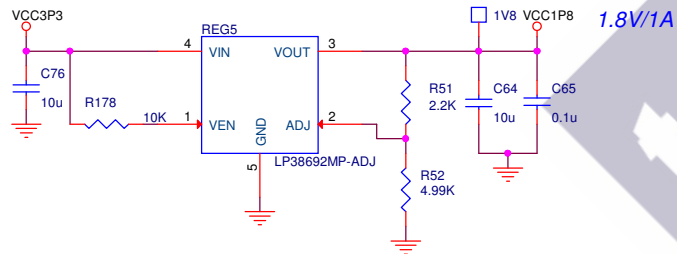
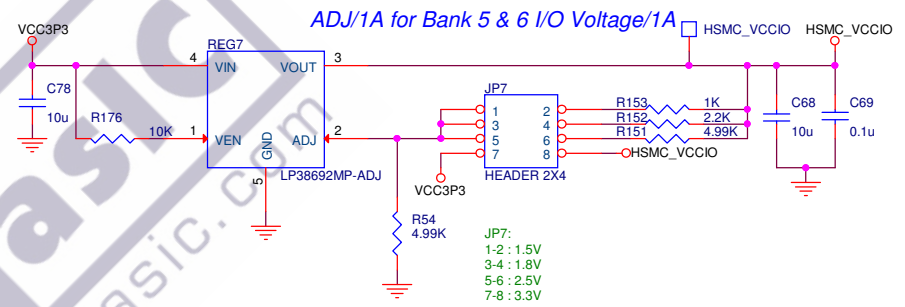
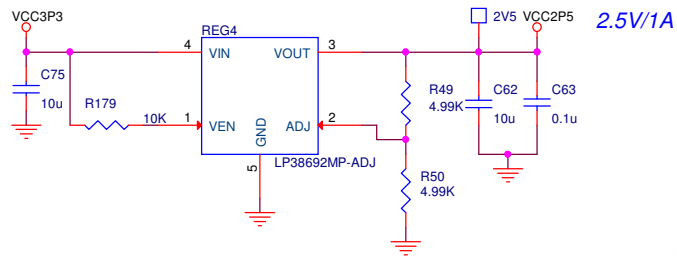
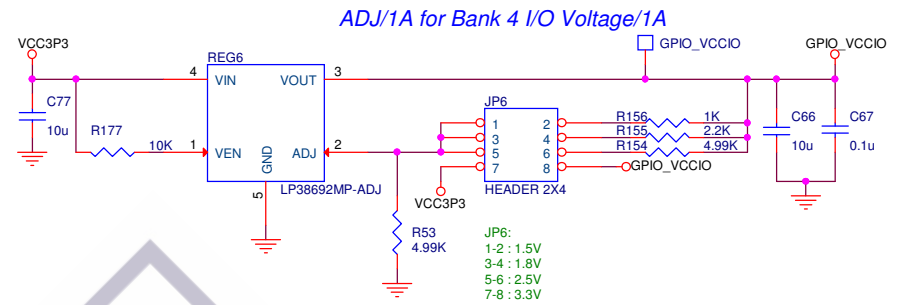
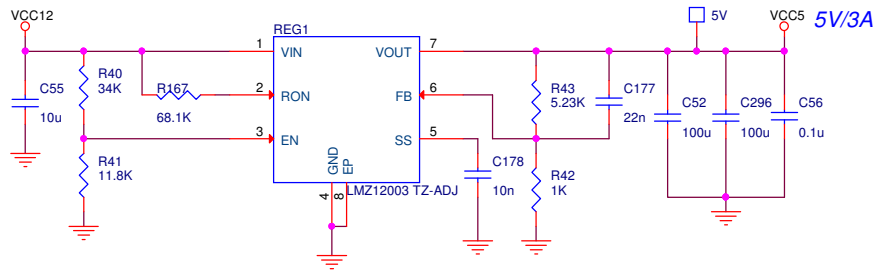


**POWER & GROUND**





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| Title   |                            |                |
| <b>DE2-115 Main Board</b>   |                            |                |
| Size  | Document Number            | Rev            |
| B   | POWER 1.2V & 3.3V          | B              |
| Date:   | Friday, September 24, 2010 | Sheet 26 of 27 |



|   |                        |
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| Title   |                        |
| <b>DE2-115 Main Board</b>   |                        |
| Size  | Document Number        |
| B   | POWER 1.8V & 2.5V & 5V |
| Date:   | Rev                    |
| Friday, September 24, 2010  | B                      |
| Sheet   | 27 of 27               |